Silicon Frontline Technology White Paper

Analyze Power Nets Early and Often with P2P

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One of the big challenges in designing ICs today is designing a robust power net capable of delivering necessary current levels to all areas of the die. Getting it wrong can, of course, lead to circuit failures that range from non-functional silicon, through intermittent performance and functional problems, to early EM-driven failures. Designers carefully perform accurate power net analysis before tapeout. However, finding problems this late in the design cycle can result in schedule slips if anything more than a trivial fix is required.

Large SoCs have complex and widely-distributed power nets, but since most of them are constructed by automated place and route they tend to have fewer late issues. They also are less amenable to early analysis since every time the design is re-placed pretty much everything changes. Furthermore, with 10 or more layers of metal, some of which are very low resistance, the problem is just not so acute.

But analog/mixed-signal ICs, memories and image sensors have many fewer layers of metal, and sometimes these are narrower (by design necessity) and of lower quality (higher resistance) materials. In addition, often these designs use complex non-orthogonal routing of power nets, which can complicate extraction and analysis for some verification tools. Obviously, eventually the power has to get down to the transistors and as a result power often has to be distributed at least partially on low levels of metal. But these low levels of metal are narrower and so resistance is more of an issue.

This is where Silicon Frontline's P2P (which stands for "point to point") comes in. It allows for extremely fast analysis of power nets very early in the design. It can even start to give preliminary analysis before the layout is complete. It does an accurate calculation of the resistance between any two points or groups of points (hence the name) with various resistance-map displays that allow the designer to quickly zoom into the issues where the resistance is very high (just look for the bright red regions in a sea of blue).

The tool is very easy to configure, very fast and has essentially unlimited capacity. Although the primary focus of the tool is not large digital SoCs, these can be handled in a few minutes to a few hours. Where the tool really shines is on analog/mixed-signal, memories, image sensors and other designs where the power nets, because of their complexity and all-angle shapes, often require manual intervention. The resistance mapping mode of P2P can be used on incomplete layouts, or during layout development in the architecture and partitioning stage of design. And then, when the design is complete and P2P resistance mapping has been used to ensure that all power nets are low resistance and any simple problems have been fixed, the designer can use P2P to perform detailed IR drop and electromigration (EM) analysis with a good candidate design. If all resistances are low then IR drop will be low (or lower) by definition and typically EM is less of an issue too, since low resistance metal tends to be wider.

The detailed IR/EM analysis can also be performed by P2P, but that is a topic for a future white paper.

So to illustrate the capabilities of P2P here is an example of its use. Some errors have been deliberately introduced since it would not be very informative if everything was perfect first time. And in IC design, nothing is ever perfect first time.

This demonstration design is an IP logic block, shown in Figure 1. It has 5 metal layers but in this example, only M1 and M2 are used for power distribution. The layout measures 1.3mmx0.8mm.

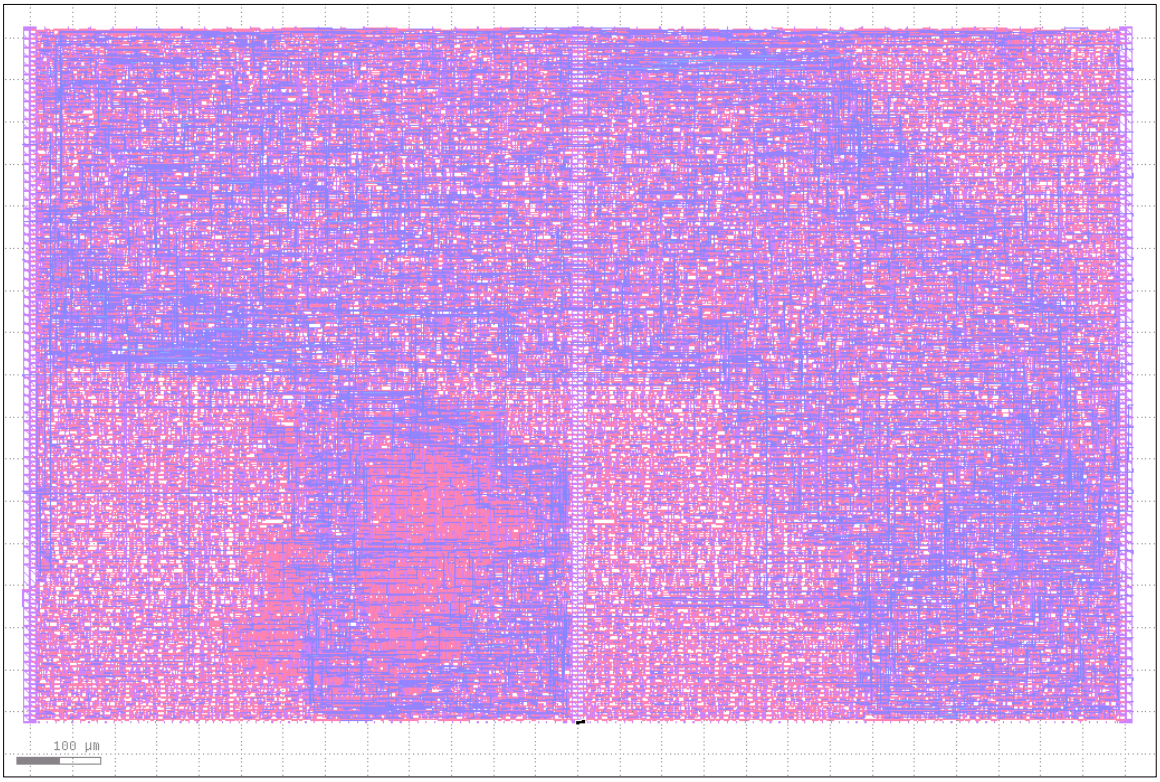

Figure 1: IP Logic Block Layout

We'll start with RMAP (resistance map) analysis of the VDD net (and VSS, not shown in this white paper). This analysis produces the "heat map" (or "resistance map", see Figure 2) showing the worst case resistance from every location on every metal layer of the VDD net to an external pin. The dark blue areas are lower resistance but the red and yellow areas are a problem. Looking to the scale on the right the darkest red is 30Ω which is much too high for such a large block.

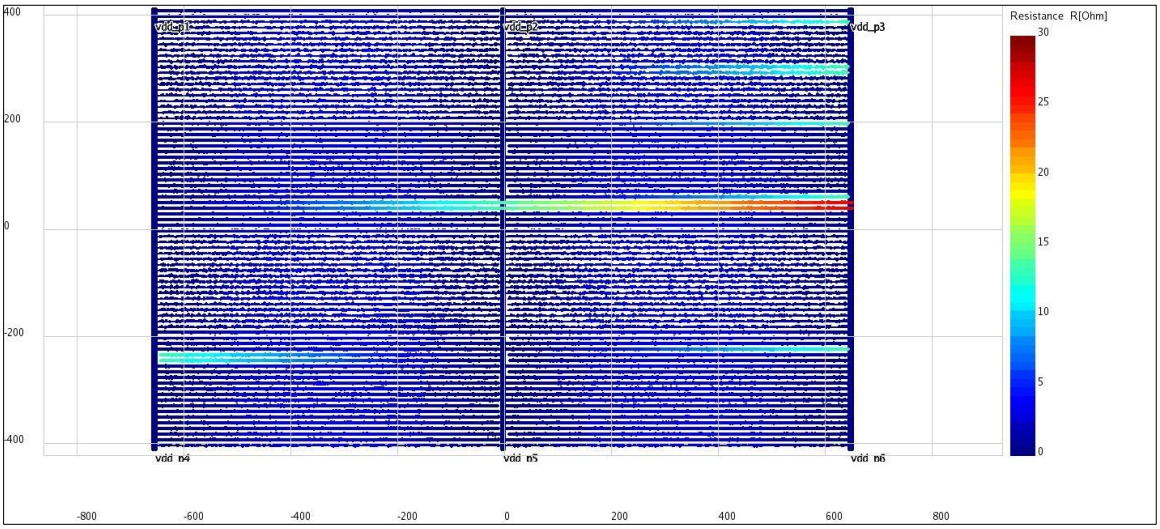

Figure 2: 1st VDD RMAP run results

Something is not right in the red area half-way up the right hand side where there is very high resistance. It is time to zoom in on that area. This does not require P2P analysis to be run again; the P2P GUI lets you zoom-in on a subset of the data. Although the absolute value of the resistance is a useful guide, in this case the diagnosis is clear when you consider resistance gradient. Viewing figure 3 you can see, over to the right of the picture, a vertical power bus (M2) in blue and horizontal red lines

(M1) indicate that there is very high resistance – this means that there is a disconnect between M1 and M2 in this location. An obvious theory is that perhaps there are too few vias.

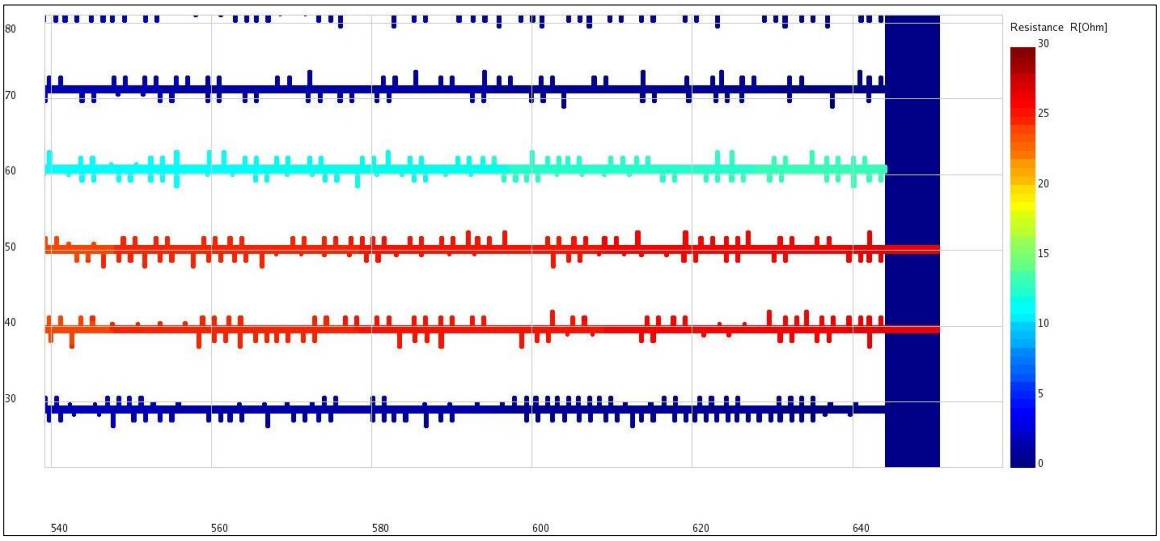

Figure 3: 1st VDD RMAP run detail

We can focus in further, see figure 4, graying out M2 (the vertical power bus) and adding vias to the display (also in grey). It is obvious what the problem is. The designer left out vias where M2 overlaps M1 in the highlighted areas so that the horizontal M1 is actually only connected at one end (far to the left, out of this picture, at the center vertical stripe).

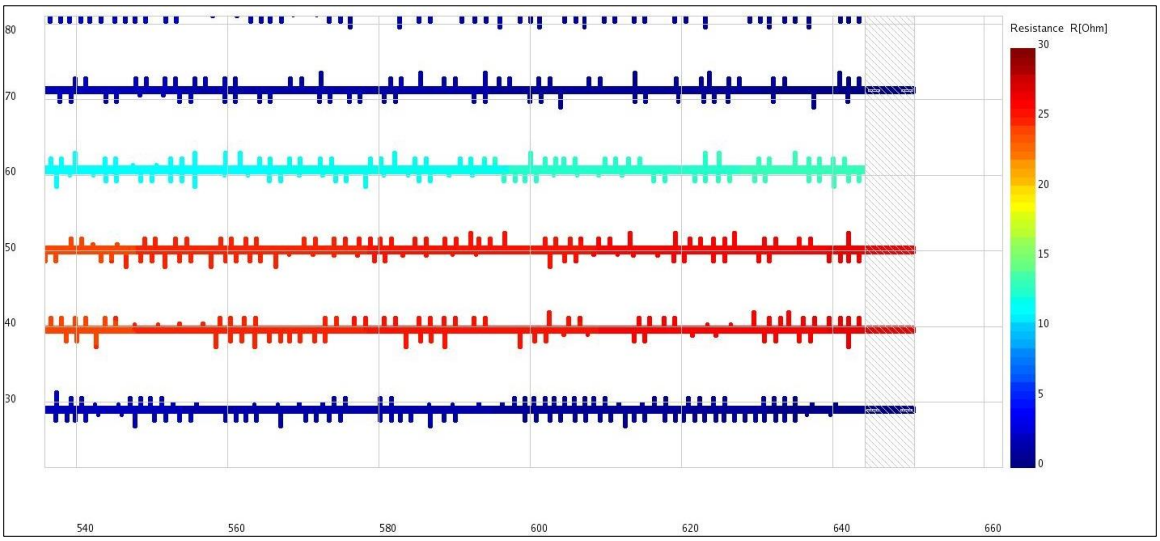

Figure 4: 1st VDD RMAP run with vias displayed

Back in the original layout, the VDD net can be updated with the added vias and the P2P analysis re-run. For this example, P2P execution is between one and two minutes. Now the RMAP looks a lot better (see figure 5 – 2nd RMAP run results) although it is not immediately obvious since there are

more red regions than previously. But the histogram scale adjusts automatically from blue to red, and red now represents only 14Ω, half what it did before.

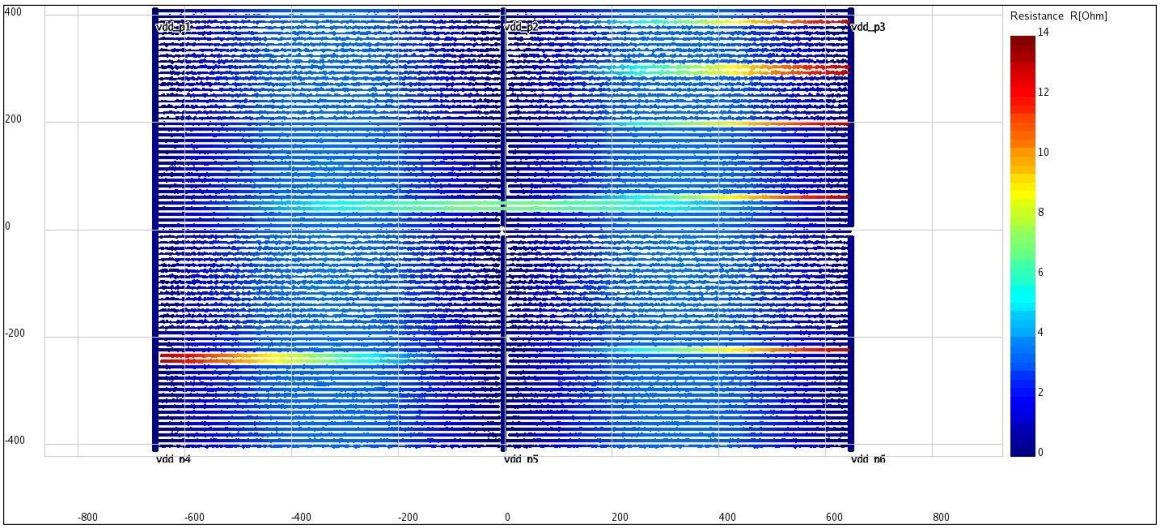

Figure 5: 2nd VDD RMAP run results

We want to get the resistance down further – we'd like to see single digit Ohms for a block of this size. If we once again zoom in (figure 6) on the area where we just added vias we can see that while we are down from two problem areas, there is still a remaining connection problem. In this case M1 doesn't extend under the M2 and so cannot be connected no matter how many vias are inserted there.

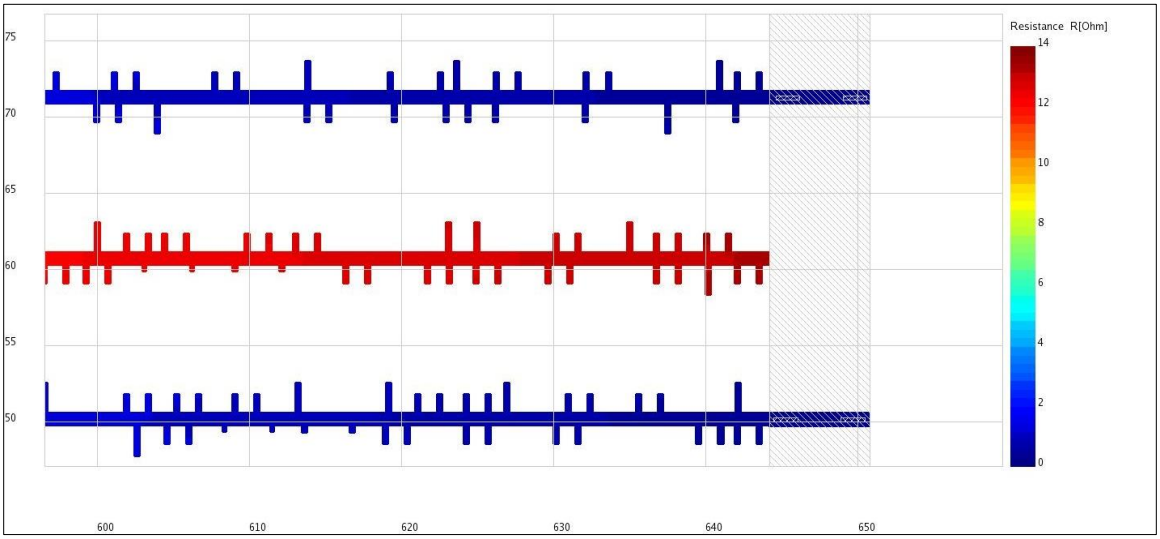

Figure 6: 2nd VDD RMAP run detail

Just visually inspecting the RMAP makes it clear that there are probably 4 other places with the same issue so they can all be fixed at once. We can then run a 3rd resistance mapping analysis, taking another minute or so, and cross our fingers that everything is now blue. Actually it will never be all blue since the highest resistance areas, no matter how low, will be colored red since the scale adjusts.

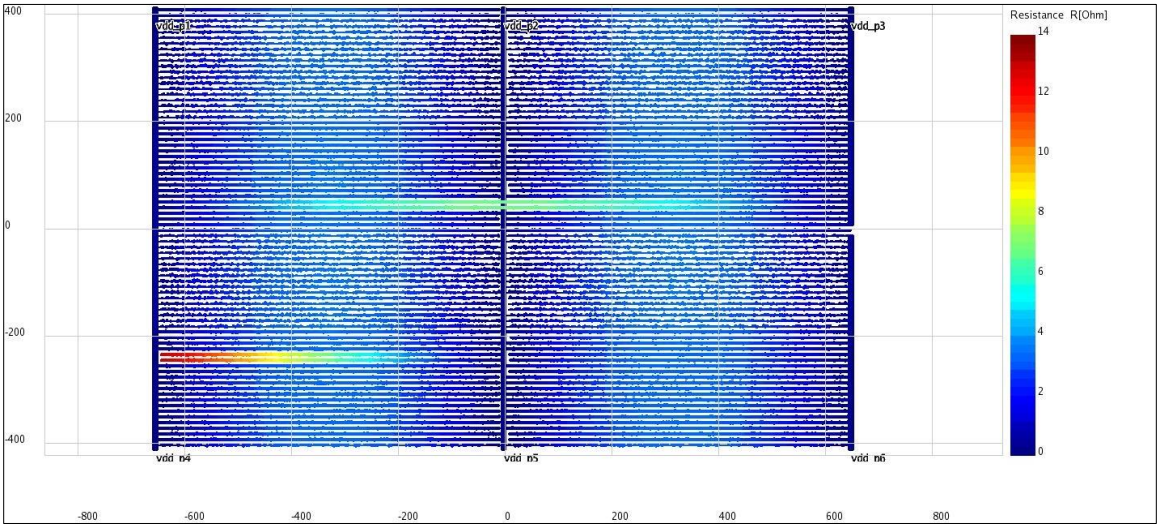

Figure 7: 3rd VDD RMAP run results

The maximum resistance is still 14Ω (see figure 7) but with the problems fixed on the right hand side it is time to see why there is a problem on the left. We can zoom in on that area (figure 8) and it is obvious that the problem is the same as on the right, the horizontal M1 does not extend far enough to reach the power bus. This would likely have been caught during a thorough review of all high resistance areas, and more easily seen by adjusting the histogram binning profile (by setting the lower limit to, say, 10Ω or 12Ω).

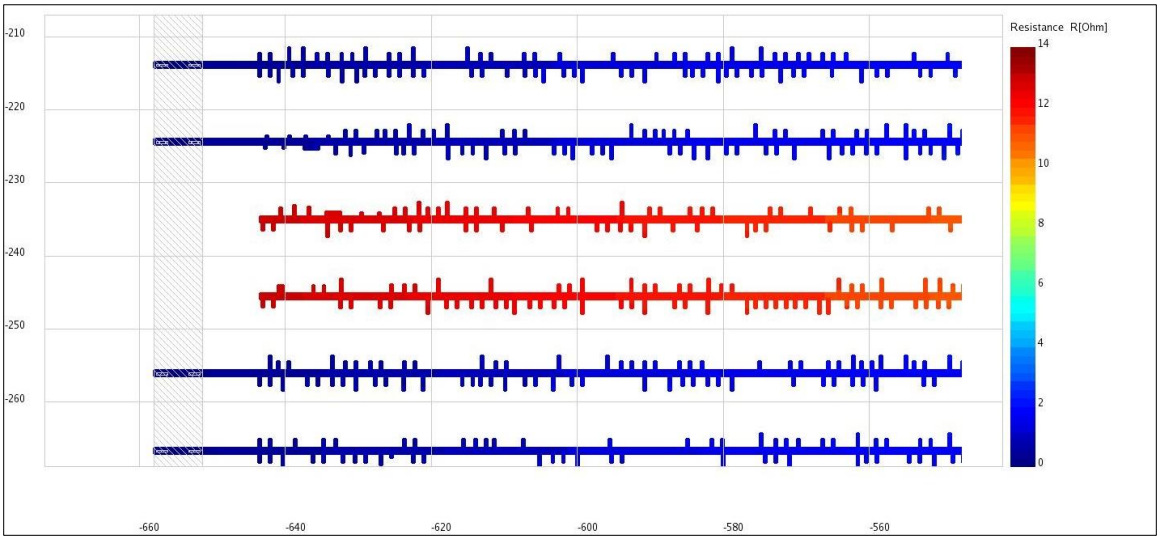

Figure 8: 3rd VDD RMAP run detail

Once that is fixed, a new run (the 4th – see figure 9) of the analysis shows that the maximum resistance is now down to 7Ω and is located in the center of the block. We can once again zoom in on the center and it is clear that once again there are no vias connecting the horizontal M1 to the vertical M2 power bus that runs through the center of the chip. We fix that, and run a 5th RMAP.

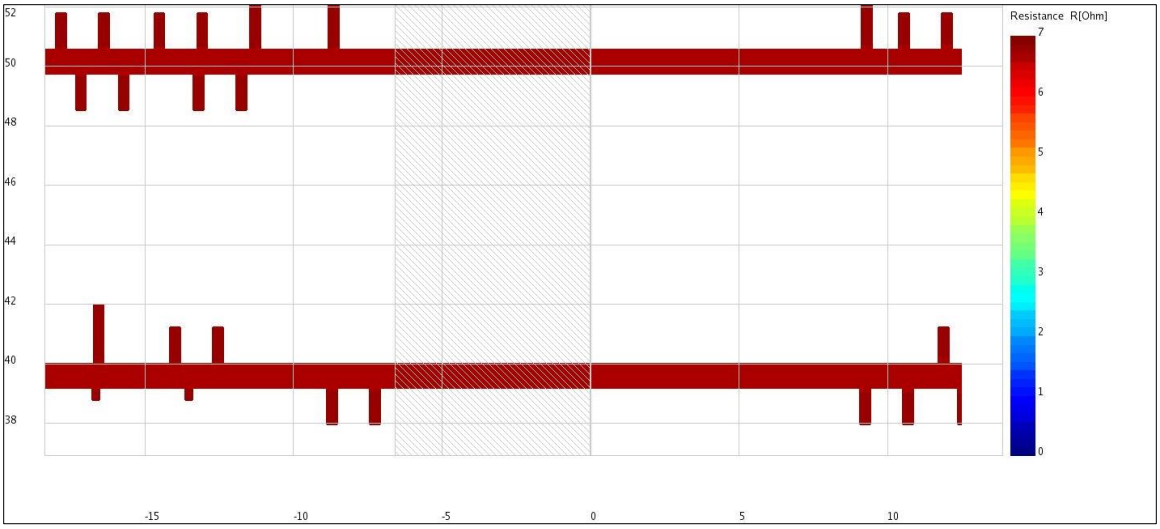

Figure 9: 4th RMAP run detail

Finally, the maximum VDD net resistance from any of the 6 external pins is around 3.5Ω (see figure 10). Remember, the scale adjusts so the sea of red is not automatically a sign of a problem. In fact, as you would expect, the resistance goes up as the horizontal nets get further away from the 3 vertical power buses. Intuitively, given the vertical M2 power routes, this is exactly the sort of map we would expect to see when everything is going right.

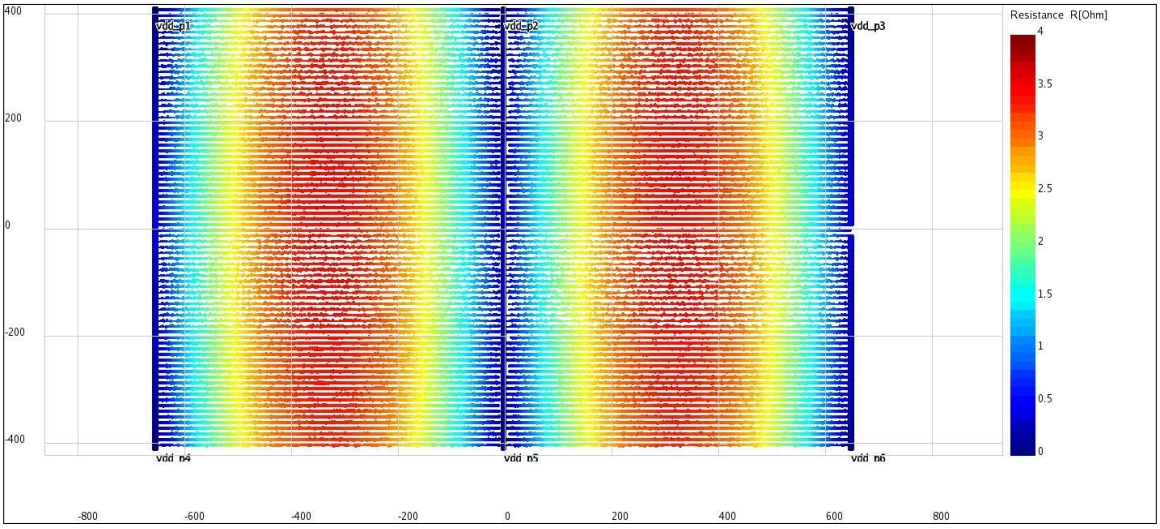

Figure 10: 5th RMAP run results

So in a matter of minutes the worst case VDD resistance has been decreased by nearly 90% from around 30Ω to 3.5Ω. Of course this example is a little contrived with very blatant errors such as omitted vias and obviously incorrect layout. Nonetheless it shows the value of doing early power analysis and fixing problems. It would have been a complete waste of time to have run a computationally expensive IR drop analysis on the original power network before these issues were addressed. And imagine how difficult it is to identify such issues in larger power nets, with more complicated structures.

P2P can also do even more detailed analysis. For example, by looking in the report file the point of greatest resistance is easily identified. Not surprisingly, it is in the very center of one of the main arrays, about as far from all the power pins as you can get. With a couple of statements we can put 0V

sources on the external pins. Drop a pin on the point of worst resistance and a current source (the value doesn't matter) on it. Then run P2P again. The pin is clearly marked in the middle of the left array. The map is now a voltage map (the earlier ones were all resistance) from zero (dark blue) to 4V (red). As is to be expected, the voltage drop to the added pin is largely on the narrower horizontal M1. Further reduction in resistance to this point would seem to require adding additional vertical M2 stripes or other more extensive layout changes.

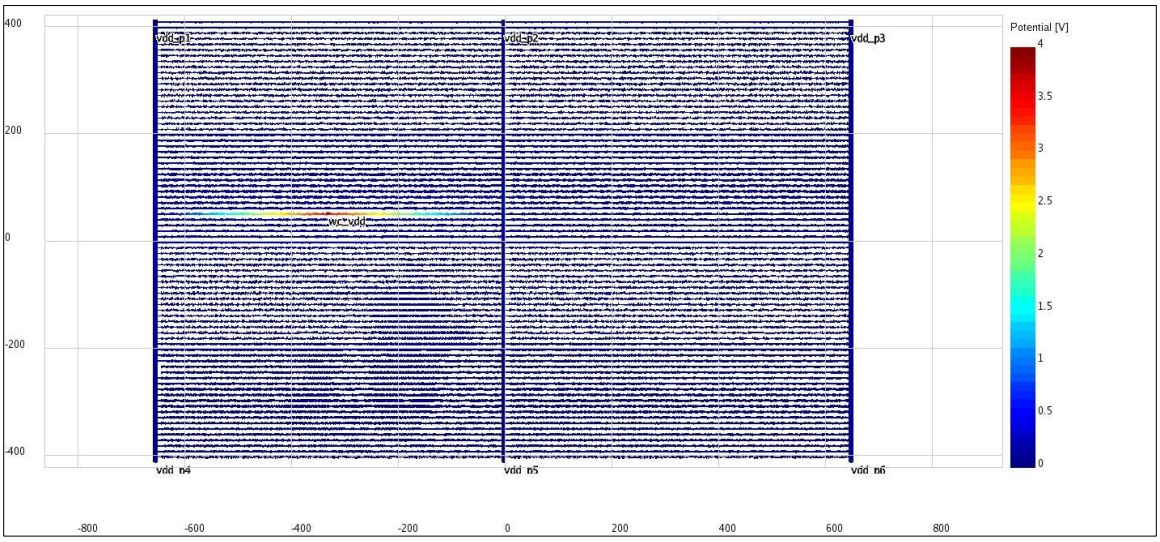

Figure 11: Voltage drop analysis results

We can also look at a current map. Now the scale is in Amps ranging from 0 (dark blue) to 1.2A (red). As you would expect since things are in pretty good shape now, the current seems evenly distributed along M2 and then M1 leading to the pin we dropped.

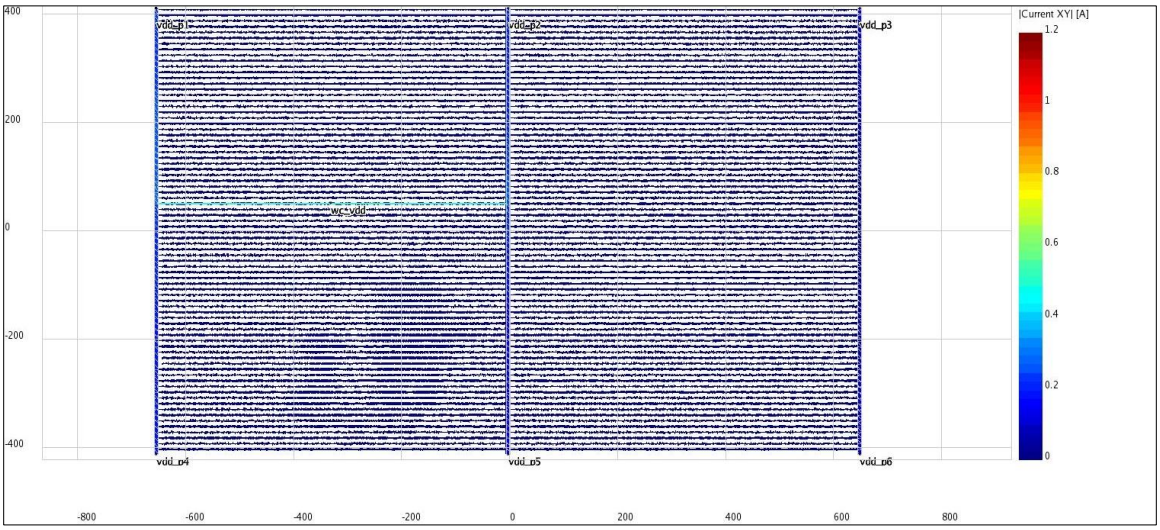

Figure 12: Current analysis results

To summarize, early and fast analysis of power networks allows problems to be identified and fixed early when they have the least impact on the schedule and also avoid unnecessary wasted runs of expensive analysis for IR and EM, or having to rip-up and reroute the power network after the design is "finished".

Resistance mapping gives a qualitative analysis that is:

- trivially easy to configure
- has capacity for the largest circuits
- runs in minutes to a few hours
- means that IR/EM analysis is done with a good candidate network
- IR/EM analysis can also be done in P2P but that will be covered in a future white paper